

# NCV7240EVB

## NCV7240 Octal Low-Side Relay Driver Evaluation Board User's Manual



ON Semiconductor®

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### EVAL BOARD USER'S MANUAL

#### Description

The NCV7240 evaluation board provides a convenient method to evaluate the NCV7240 octal low-side driver in a customer defined application environment.

The setup involves the use of a PC installed with custom designed software, an interface board, and the NCV7240 evaluation board. The evaluation board is controlled using the ON Semiconductor FlexMOS GUI installed on a personal computer (PC). The USB to SPI interface adapter board provides master-slave communication between the target demonstration board and the PC.

The user can control each of the eight low-side outputs independently using this system setup.

The evaluation board's power management includes an adjustable LDO giving the option for a 3.3 V or 5 V digital supply voltage (VCC) selectable through the GUI. An external power supply can be used by removing a jumper on the board. Visual indicators dictate the board configuration through LEDs.

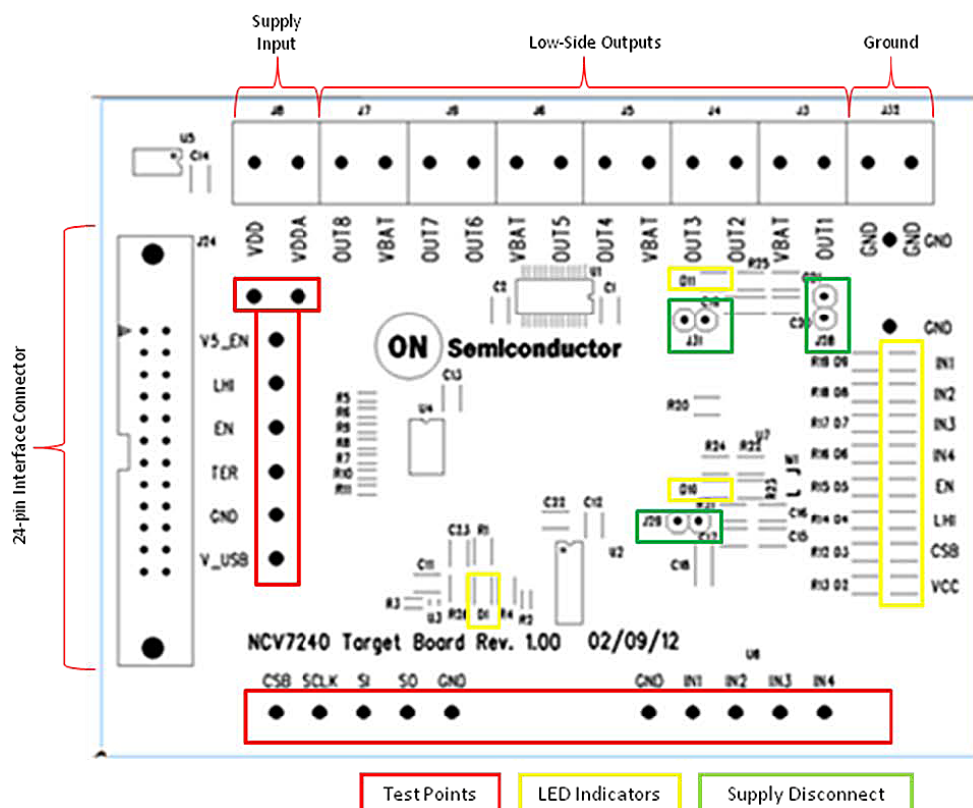
#### Features

- 8 Channels
- 600 mA Low-Side Drivers
- Programmable Logic Supply Voltage
- 16-bit SPI Control
- Over Load and Over Temperature Protection
- Selectable Open Load Detection for LED Loads
- Dedicated GUI Interface for Device Control and Diagnostic



Figure 1. Evaluation Board Solution

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### Figure 2. Evaluation Board

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Rating                                      | Value       | Units |
|---------------------------------------------|-------------|-------|
| Main Supply Voltage to output pins (OUTx)   | −0.3 to 36  | V     |
| Digital Supply Voltage (VCC)                | −0.3 to 5.5 | V     |
| USB to SPI Interface Adapter Connector Pins | −0.5 to 5.5 | V     |
| Junction Temperature (NCV7240)              | −40 to 150  | °C    |
| Ambient Temperature (Evaluation board)      | −40 to 105  | °C    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Table 2. RECOMMENDED OPERATING CONDITIONS

| Rating                                | Value |     | Units |
|---------------------------------------|-------|-----|-------|
|                                       | Min   | Max |       |
| External Digital Supply Voltage (VCC) | 3.0   | 5.5 | V     |
| Main Supply Voltage (VBAT)            | 5.5   | 28  | V     |
| DC Output Current                     | –     | 0.6 | A     |
| Junction Temperature                  | –40   | 125 | °C    |

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**Table 3. PIN FUNCTION DESCRIPTION**

| Connector                  | Pin Number | Terminal Name | Description                                                                            |
|----------------------------|------------|---------------|----------------------------------------------------------------------------------------|
| 24 Pin Interface Connector | 1          | SCL           | I2C Clock Line, 3.3 V Levels                                                           |
|                            | 2          | SDA           | I2C Data Line, 3.3 V Levels                                                            |
|                            | 3          | GND           | Ground                                                                                 |
|                            | 4          | GND           | Ground                                                                                 |
|                            | 5          | IN4           | General-Purpose Output 7, used for parallel control of OUT4 and OUT8                   |
|                            | 6          | PO6           | General-Purpose Output 6                                                               |
|                            | 7          | IN3           | General-Purpose Output 5, used for parallel control of OUT3 and OUT7                   |
|                            | 8          | V5_EN         | General-Purpose Output 4, used for controlling the LDO reference                       |
|                            | 9          | IN2           | General-Purpose Output 3, used for parallel control of OUT2 and OUT6                   |
|                            | 10         | IN1           | General-Purpose Output 2, used for parallel control of OUT1 and OUT5                   |
|                            | 11         | EN            | General-Purpose Output 1, used for EN, Chip Enable                                     |
|                            | 12         | LHI           | General-Purpose Output 0, used for Limp-Home Logic input                               |
|                            | 13         | GND           | Ground                                                                                 |
|                            | 14         | GND           | Ground                                                                                 |
|                            | 15         | PI1           | General-Purpose Input 1                                                                |
|                            | 16         | PI0           | General-Purpose Input 0                                                                |
|                            | 17         | VIO           | 3.3 V or 5 V for level translators                                                     |
|                            | 18         | PI2           | General-Purpose Input 2                                                                |
|                            | 19         | SO            | SPI data from slave to master                                                          |
|                            | 20         | SI            | SPI data from master to slave                                                          |
|                            | 21         | SCLK          | SPI clock from master to slave                                                         |
|                            | 22         | CSB           | SPI slave chip select bar                                                              |
|                            | 23         | VTRGT         | 5 V Supply from slave to J1                                                            |
|                            | 24         | VCC_USB       | 5 V USB voltage from the USB to SPI adapter board to the evaluation board (100 mA max) |
| Supply Requirement         |            | VBAT          | Main Supply Voltage. Powers the NCV7240 drivers and the onboard LDO.                   |
|                            |            | GND           | Ground                                                                                 |
| Low_Side Driver Outputs    |            | OUT1          | Low-Side Output 1                                                                      |
|                            |            | OUT2          | Low-Side Output 2                                                                      |
|                            |            | OUT3          | Low-Side Output 3                                                                      |
|                            |            | OUT4          | Low-Side Output 4                                                                      |
|                            |            | OUT5          | Low-Side Output 5                                                                      |
|                            |            | OUT6          | Low-Side Output 6                                                                      |
|                            |            | OUT7          | Low-Side Output 7                                                                      |
|                            |            | OUT8          | Low-Side Output 8                                                                      |

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**Table 3. PIN FUNCTION DESCRIPTION**

| Connector                   | Name  | Description                                                                                                                               |
|-----------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| Test Points & LED Indicator | V5_EN | When this signal is high the LDO is programmed for 5 V output.                                                                            |
|                             | EN    | Enable signal for the integrated driver. EN LED is illuminated when the part is enabled.                                                  |
|                             | TSD   | Latched thermal information.                                                                                                              |
|                             | LHI   | Limp-Home Logic Input.                                                                                                                    |
|                             | IN1   | Parallel input 1 used for parallel control of OUT1 and OUT5. An LED is illuminated when the pin is high.                                  |
|                             | IN2   | Parallel input 2 used for parallel control of OUT2 and OUT6. An LED is illuminated when the pin is high.                                  |
|                             | IN3   | Parallel input 3 used for parallel control of OUT3 and OUT7. An LED is illuminated when the pin is high.                                  |
|                             | IN4   | Parallel input 4 used for parallel control of OUT4 and OUT8. An LED is illuminated when the pin is high.                                  |
|                             | CSB   | Chip Select Bar signal produced by the master. CSB LED is illuminated when CSB transition to a low state.                                 |
|                             | SCLK  | Serial clock signal generated by the master.                                                                                              |
|                             | SI    | Serial input data from the master.                                                                                                        |
|                             | SO    | Serial output data from the slave.                                                                                                        |
|                             | VCC   | Digital Supply voltage. VCC LED is illuminated when the LDO is regulating.                                                                |
|                             | GND   | Chip Ground                                                                                                                               |
| Supply Disconnect           | J28   | J28 disconnects the VBAT supply from the board. No power is delivered to the LDOs when the jumper is disconnected.                        |
|                             | J29   | J29 disconnects VDD supply from the LDO to the board. When the jumper is disconnected, the board can be powered from an external supply.  |
|                             | J31   | J31 disconnects VDDA supply from the LDO to the board. When the jumper is disconnected, the board can be powered from an external supply. |

## OPERATIONAL GUIDELINES

The material necessary to successfully use the evaluation boards is listed below:

- PC running the latest Onsemi FlexMOS GUI
- USB cable Type A to Type B
- USB to SPI Interface Adapter with Ribbon Cable
- NCV7240 Evaluation Board
- Power Supply
- Resistive, LED, Inductive or Motor Load

An application example of the NCV7240 driving relays is shown in Figure 3. Figure 3 shows J28, J29 and J31 jumpers

inserted. This powers the on-board LDO regulators for VDD and VDDA. Both VDD and VDDA light their respective LED (D10 and D11) when powered. The multiple VBAT connectors on the terminal blocks help the user connect loads in the system by providing a connection which provides capability for two wires per terminal site.

When VBAT voltage is applied to the board, the onboard regulator regulates the VDD voltage. By default, VCC is regulated to 3.3 V, but this can be adjusted to 5 V via the GUI.

VCC power to the board is provided via VDDA through R20 and is shown active with diode D2.

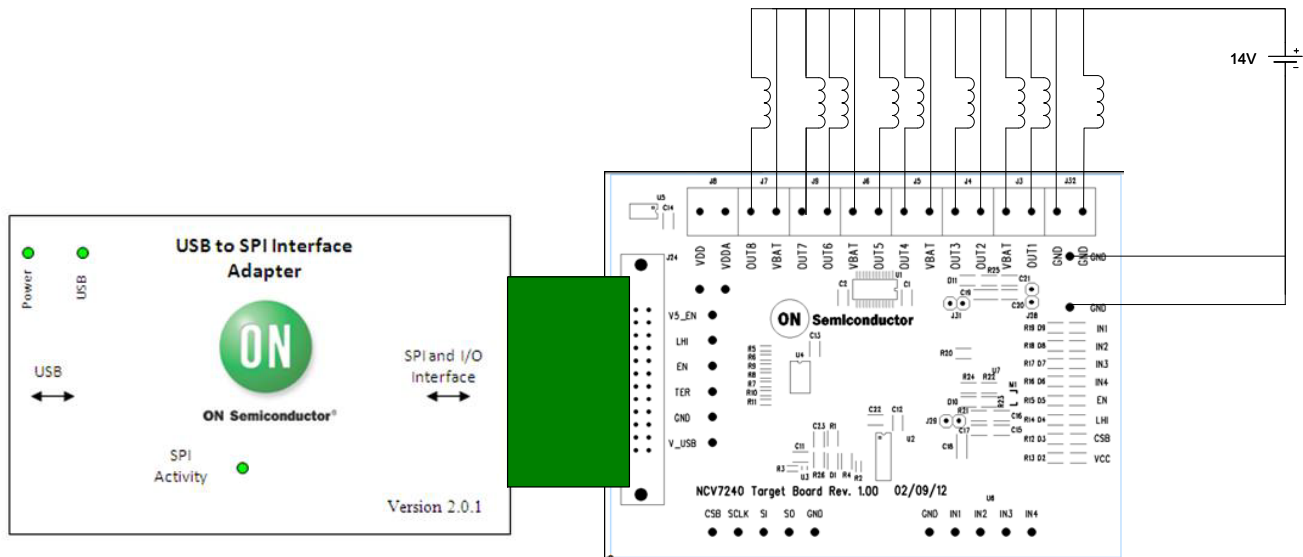


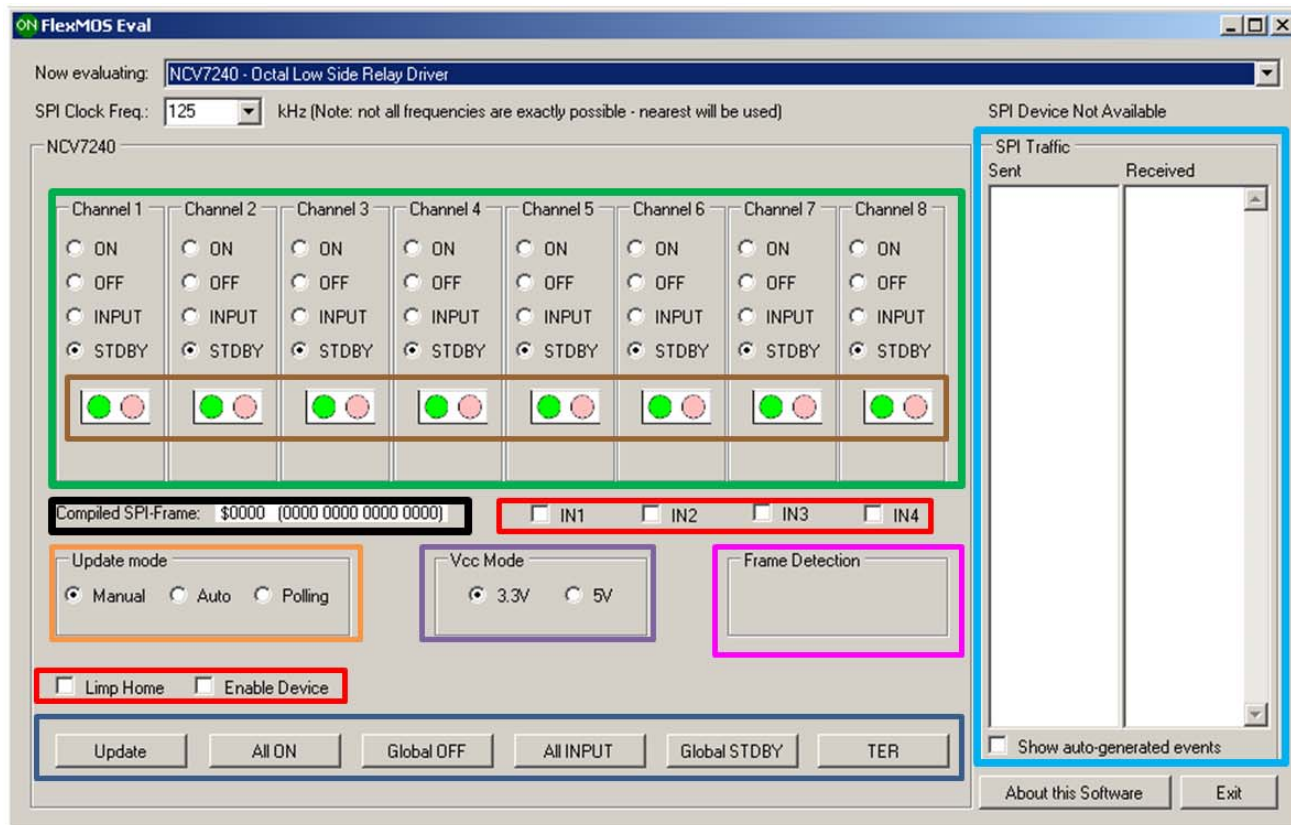
Figure 3. Application Example

Once the hardware is configured with the desired load and is interfaced with the USB to SPI adapter, the user can launch the FlexMOS software. Once the software is running, the GUI should automatically identify the connected demonstration board and load the appropriate GUI interface for the low-side drivers. If the software doesn't recognize the connected demonstration board, manually select the

device from the drop down box. If the device name doesn't appear in the drop down box, the latest version of the GUI needs to be installed on the PC.

A detailed description of the GUI functionality for the NCV7240 is shown in Figure 4. The FlexMOS GUI is used to enable or disable the device and to control the low-side driver outputs.

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**Low-Side Drive Channel Control**  
Allows independent control of each low-side driver

**Output Status**  
Displays the current status of each low-side driver.

**Compiled SPI-Frame**  
Compiled SPI frame based on the Control Input

**GUI Update Mode**  
Manual: User must press "Update" button for any changes made to Low-Side Channel Control to take effect.  
Auto: When the Low-Side Channel Control is changed the "Update" button is automatically triggered.  
Polling: the Low-side Channel Control is updated periodically at a predefined interval. This will show a constant flow of data in the SPI Traffic box.

**VCC Mode**  
Programs the onboard LDO for either 3.3V or 5V.

**Frame Detection**  
Displays results from TER or SPI command equivalent.

**SPI Traffic**  
Log of SPI commands send and received

**Push Button Control**  
Update: Transmits the compiled SPI-Frame to the slave device  
AllON: Turns all 8 low-side drivers on.  
GlobalOff: Turns all 8 low-side drivers off.  
All INPUT: Configures IN1-IN4 active.  
Global STDY: All outputs off.  
Open circuit diagnostic currents off.  
TER: Retrieves Transmission Error information.  
Displayed in Frame Detection box.

**Check Box Control**  
Enable Device: Enables or disables the integrated driver  
Limp Home: Activates channels 1-4 as per the datasheet  
INx: Parallel input pair control. See datasheet for details.

Figure 4. GUI Overview

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## TYPICAL CHARACTERISTICS

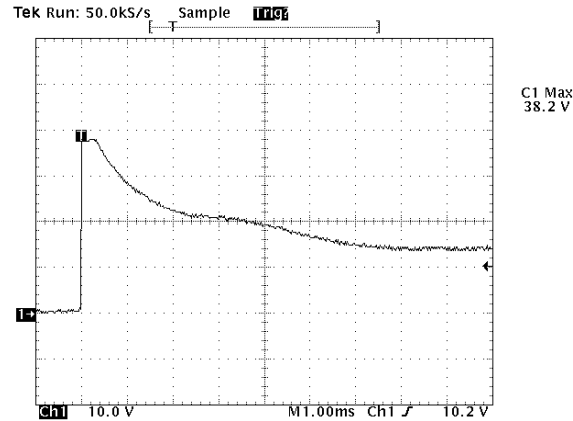


Figure 5. Typical Output Clamping Action

### Typical Operation

Figure 5 above highlights the clamping action (clamped to 38.2 V) of the NCV7240 as the device turns off when driving an inductive load. In this case, a relay has turned off. The slight hump in the decaying waveform is caused from the mechanical relay action of the system.

### Transmission Error (TER)

The NCV7240 device includes a transmission error detection feature whereby a transmission error (bit count not

a multiple of 8 [16 bit minimum]) is reported on the SO pin after CSB goes low until the first rising edge of SCLK. Detection can be performed by clicking on the TER button in the GUI.

Since SI is OR'd with the TER fault, it is important to understand that if the LSB bit (B0) is set high on the previous frame, the TER should be ignored. This is because SI holds the value of B0 until the first SCLK rising edge and TER is latched in before the first rising edge of SCLK.

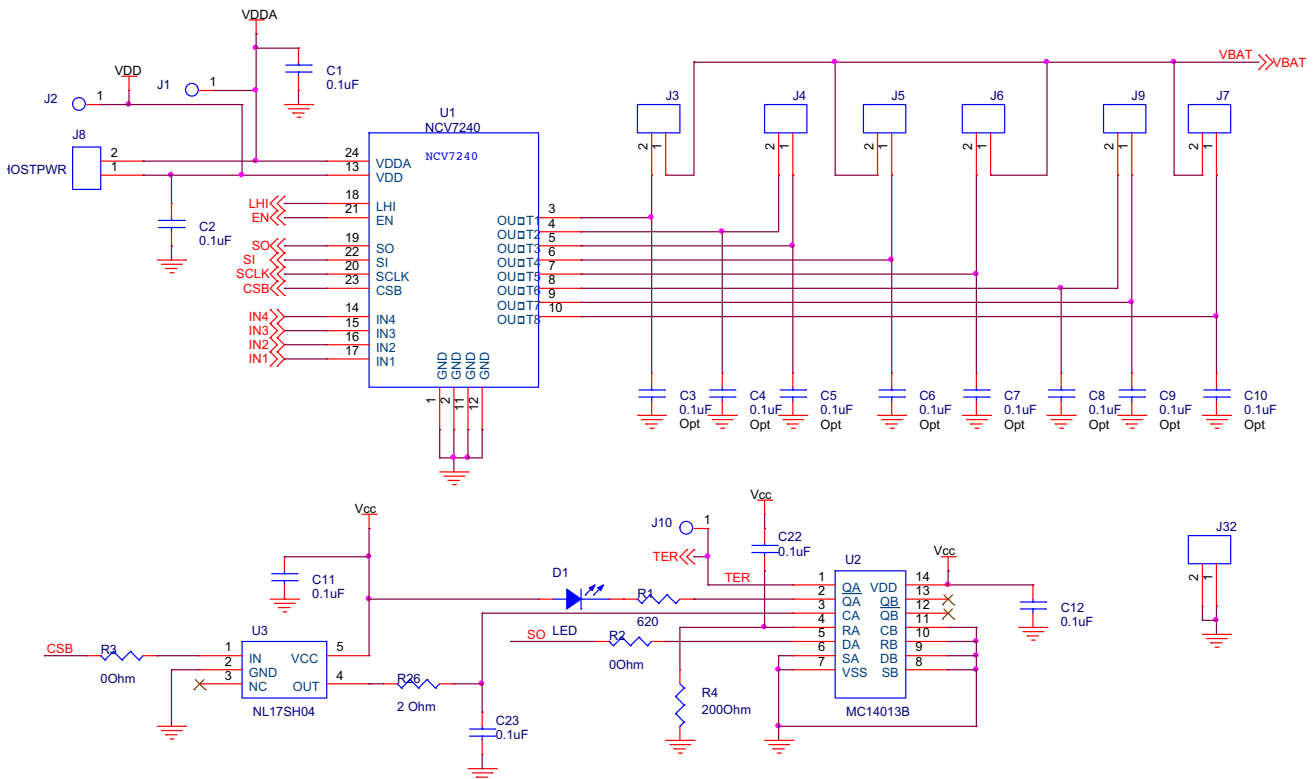


Figure 6. Evaluation Board (DUT)

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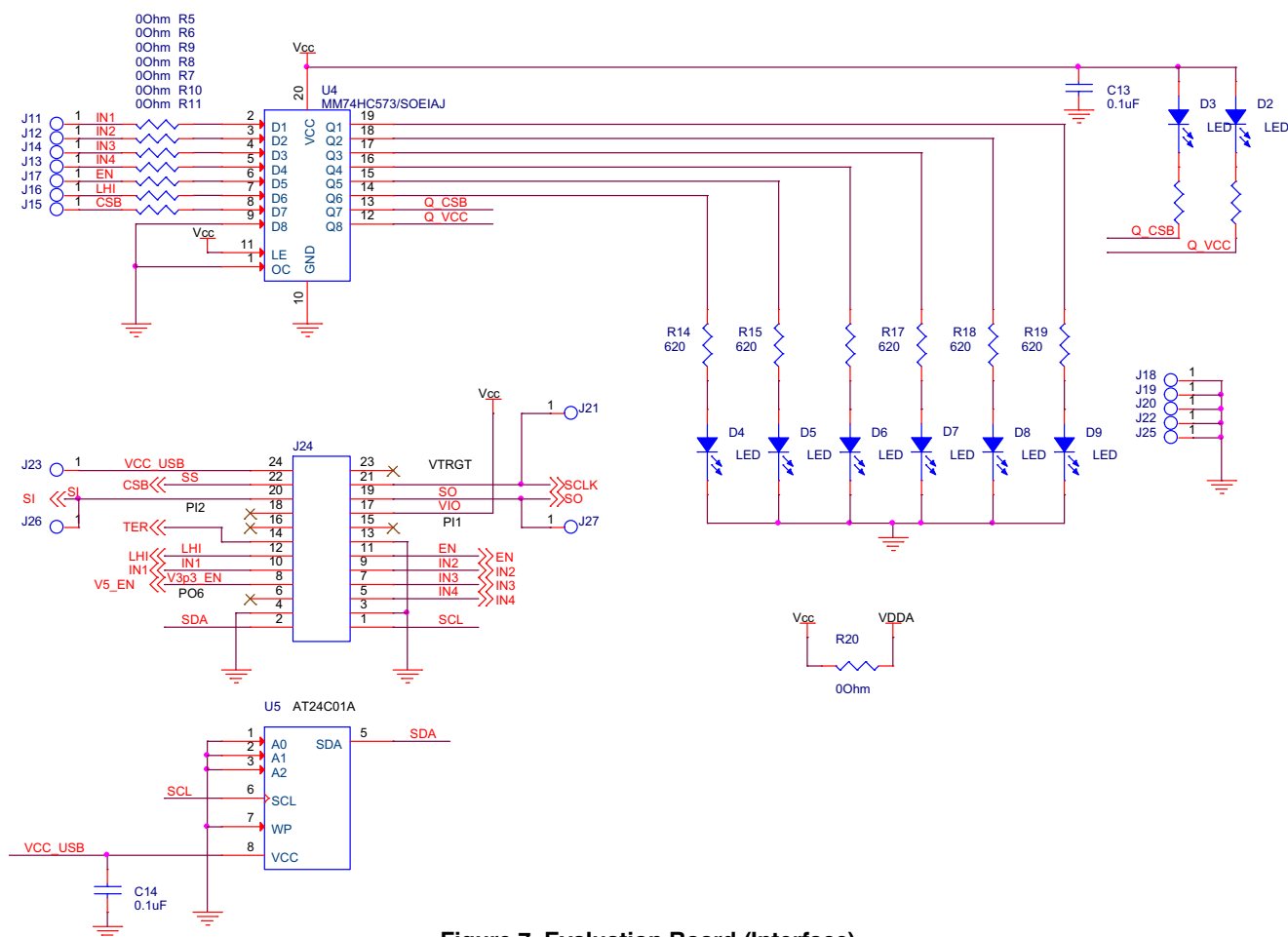


**Figure 7. Evaluation Board (Interface)**

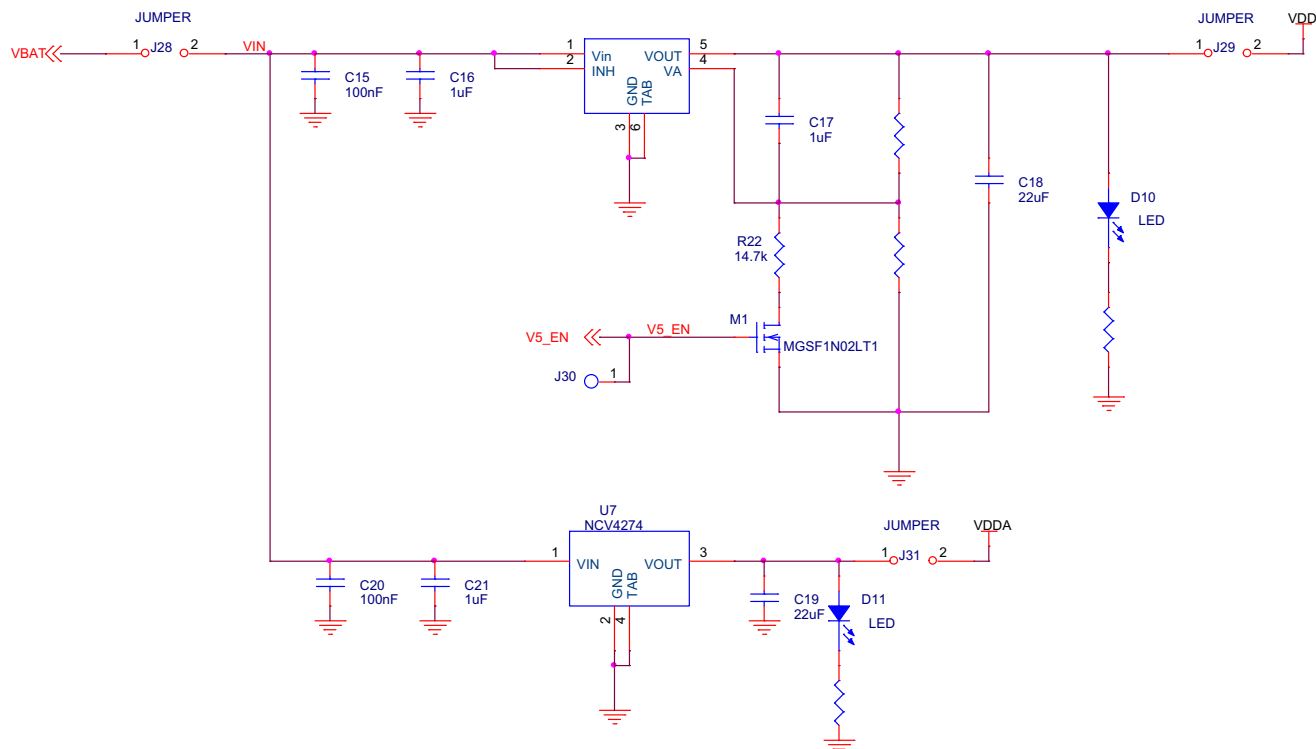


**Figure 8. Evaluation Board (Power)**

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## Bill of Materials (NCV7240 Evaluation Board)

| Reference Designator(s)                  | Quantity | Description                      | Value       | Tolerance | Footprint   | Manufacturer                     | Manufacturer's Part Number | Substitution Allowed | RoHS Compliant |
|------------------------------------------|----------|----------------------------------|-------------|-----------|-------------|----------------------------------|----------------------------|----------------------|----------------|
| C1 thru C15, C20, C22, C23               | 18       | CAP CER .1UF 50V 10% X7R 0805    | 0.1uF       | 10%       | 805         | Murata Electronics North America | GRM21BR71H104KA01L         | Yes                  | Yes            |
| C18, C19                                 | 2        | CAP CER 22UF 16V X5R 1206        | 22uF        | 20%       | 1205        | Murata Electronics North America | GRM31CR61C226ME15L         | Yes                  | Yes            |
| D1 thru D11                              | 11       | LED GREEN CLEAR THIN 0805 SMD    | N/A         | N/A       | 805         | Lite-On Inc                      | LTST-C171GKT               | Yes                  | Yes            |
| J1, J2, J10 thru J23, J25, J26, J27, J30 | 20       | TEST POINT PC MULTI PURPOSE RED  | N/A         | N/A       | TP          | Keystone Electronics             | 5010                       | Yes                  | Yes            |
| J3 thru J9, J32                          | 8        | CONN TERM BLOCK 2POS 5.08MM PCB  | N/A         | N/A       | MKDSN2      | Phoenix Contact                  | 1729128                    | No                   | Yes            |
| J24                                      | 1        | CONN HEADER VERT 24POS .100 GOLD | N/A         | N/A       | FRC24_VE RT | TE Connectivity                  | 5499910-5                  | No                   | Yes            |
| J28, J29, J31                            | 3        | CONN HEADER 2POS .100 VERT GOLD  | N/A         | N/A       | JMP         | Molex Connector Corporation      | 22-28-4024                 | Yes                  | Yes            |
| M1                                       | 1        | MOSFET N-CH 20V 750MA SOT23      | 20V / 0.75A | N/A       | SOT23       | ON Semiconductor                 | MG5F1N02LT1G               | No                   | Yes            |
| R1, R12 thru R19, R24, R25               | 11       | RES 620 OHM 1/8W 1% 0805 SMD     | 620         | 1%        | 805         | Vishay/Dale                      | CRCW0805620RFKEA           | Yes                  | Yes            |
| R2, R3, R5 thru R11                      | 9        | RES 0.0 OHM 1/10W 0503 SMD       | 0           | Jumper    | 603         | Panasonic- ECG                   | ERJ-3GEY0R00V              | Yes                  | Yes            |
| R4                                       | 1        | RES 200 OHM 1/8W 1% 0805 SMD     | 200         | 1%        | 805         | Vishay/Dale                      | CRCW0805200RFKEA           | Yes                  | Yes            |
| R20                                      | 1        | RES 0.0 OHM 1/8W 0805 SMD        | 0           | Jumper    | 805         | Vishay/Dale                      | CRCW08050000Z0EA           | Yes                  | Yes            |
| R21                                      | 1        | RES 10.0K OHM 1/8W 1% 0805 SMD   | 10.0K       | 1%        | 805         | Vishay/Dale                      | CRCW080510K0FKEA           | Yes                  | Yes            |
| R22                                      | 1        | RES 14.7K OHM 1/8W 1% 0805 SMD   | 14.7K       | 1%        | 805         | Vishay/Dale                      | CRCW080514K7FKEA           | Yes                  | Yes            |
| R23                                      | 1        | RES 30.9K OHM 1/8W 1% 0805 SMD   | 30.9K       | 1%        | 805         | Vishay/Dale                      | CRCW080530K9FKEA           | Yes                  | Yes            |
| R26                                      | 1        | RES 2.00 OHM 1/8W 1% 0805 SMD    | 2           | 1%        | 805         | Vishay/Dale                      | CRCW08052R00FKEA           | Yes                  | Yes            |
| U1                                       | 1        | Octal Low-Side Relay Driver      | N/A         | N/A       | SSOP24      | ON Semiconductor                 | NCV7240DPR2G               | No                   | Yes            |
| U2                                       | 1        | IC FLIP-FLOP DUAL CMOS 14SOIC    | N/A         | N/A       | SOIC14_N    | ON Semiconductor                 | MC140138DR2G               | No                   | Yes            |
| U3                                       | 1        | Single Inverter                  | N/A         | N/A       | SOT-953     | ON Semiconductor                 | NL17SH04P5T5G              | No                   | Yes            |
| U4                                       | 1        | IC LATCH OCTAL D 3STATE 20-TSSOP | N/A         | N/A       | TSOP-20-2   | ON Semiconductor                 | MC74HC573ADTG              | No                   | Yes            |
| U5                                       | 1        | IC EEPROM 1KBIT 1M-HZ 8SOIC      | N/A         | N/A       | SOIC8_N     | ON Semiconductor                 | CAT93C56VI-GT3             | No                   | Yes            |
| U6                                       | 1        | IC REG LDO 400MA ADJ D-PAK       | N/A         | N/A       | DPAK5       | ON Semiconductor                 | NCV4276BDTADJRKG           | No                   | Yes            |
| U7                                       | 1        | IC REG LDO 400MA 5.0V DPAK       | N/A         | N/A       | DPAK3       | ON Semiconductor                 | NCV4274ADT50RKG            | No                   | Yes            |

## EVALUATION BOARD LAYOUT



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